WHAT WE CLAIM ARE:

1. A manufacture method for a thin film transistor substrate, comprising the steps of:

(a) forming a semiconductor layer on a substrate, said semiconductor layer having a threshold voltage suitable for an n-channel transistor;

(b) pattering said semiconductor layer into island areas by using a first mask to define an area of a pixel driving n-channel transistor with LDD regions, an area of a CMOS n-channel transistor and an area of a CMOS p-channel transistor;

(c) forming a gate insulating film and a first gate electrode layer to cover said semiconductor layer patterned to form the island areas;

(d) patterning said first gate electrode layer by using a second mask to form a first gate electrode layer having an opening in the CMOS p-channel transistor area;

(e) by using said first gate electrode layer as a mask, implanting n-type impurity ions into the CMOS p-channel transistor area in the opening to set a threshold voltage suitable for the CMOS p-channel transistor;

(f) after said step (e), forming a second gate electrode layer covering said first gate electrode layer;

(g) etching said second gate electrode layer by using a third mask to form second gate electrodes having a gate electrode shape;

(h) by using said second gate electrodes and said first gate electrode layer as a mask, implanting high concentration p-type impurity ions into the CMOS p-channel transistor area to form high impurity concentration

source/drain regions;

(i) by using said second gate electrodes as a mask, etching said first gate electrode layer to form gate electrodes of the n-channel transistors;

(j) by using a fourth mask covering the CMOS p-channel transistor area and the LDD regions in the area of the n-channel transistor with the LDD regions, implanting high concentration n-type impurity ions to form high impurity concentration source/drain regions of the n-channel transistors; and

(k) implanting low concentration n-type impurity ions to form the LDD regions in the area of the n-channel transistor with the LDD regions.

2. The manufacture method for a thin film transistor substrate according to claim 1, wherein the CMOS n-channel transistor has no LDD regions and said fourth mask has an opening corresponding to the MOS n-channel transistor area.

3. The manufacture method for a thin film transistor substrate according to claim 1, wherein said step (a) comprises the subsidiary steps of:

(a1) depositing said semiconductor layer on the substrate in an amorphous phase;

(a2) implanting p-type impurity ions into said semiconductor layer at an impurity concentration which sets the threshold voltage suitable for the n-channel transistor; and

(a3) applying a laser beam to said semiconductor layer to change the amorphous phase to a polycrystallized phase.

4. The manufacture method for a thin film transistor substrate according to

claim 1, wherein said first and second gate electrode layers have different etching characteristics.

5. The manufacture method for a thin film transistor substrate according to claim 1, wherein said first gate electrode layer is a refractory metal layer and said second gate electrode layer is an aluminum alloy layer.

6. The manufacture method for a thin film transistor substrate according to claim 1, further comprising the steps of:

(l) forming a first interlayer insulating film covering said three types of thin film transistor structures;

(m) forming contact holes through said first interlayer insulating film and said gate insulating film;

(n) forming a conductive layer on said first interlayer insulating film, said conductive layer covering said contact holes;

(o) pattering said conductive layer to form electrodes and wiring lines;

(p) forming a second interlayer insulating film covering said electrodes and said wiring lines;

(q) forming contact holes through said second interlayer insulating film;

(r) forming a transparent electrode layer on said second interlayer insulating film, said transparent electrode layer covering said contact holes; and

(s) patterning said transparent electrode layer to form a transparent electrode of each pixel.

7. A manufacture method for a thin film transistor substrate, comprising the steps of:

(a) forming a semiconductor layer on a substrate, said semiconductor layer having a threshold voltage suitable for a p-channel transistor;

(b) pattering said semiconductor layer into island areas by using a first mask to define an area of a pixel driving n-channel transistor with LDD regions, an area of a CMOS n-channel transistor and an area of a CMOS p-channel transistor;

(c) forming a gate insulating film and a first gate electrode layer to cover said semiconductor layer patterned to form the island areas;

(d) patterning said first gate electrode layer by using a second mask to form a first gate electrode layer covering the CMOS p-channel transistor area and having an opening in the n-channel transistor areas;

(e) by using said first gate electrode layer as a mask, implanting p-type low concentration impurity ions into the n-channel transistor areas in the opening to set a threshold voltage suitable for the n-channel transistors;

(f) after said step (e), forming a second gate electrode layer covering said first gate electrode layer;

(g) etching said second gate electrode layer by using a third mask to form a second gate electrode layer having a gate electrode shape covering a channel region and the LDD regions in the area of the n-channel transistor with the LDD regions and having a gate electrode shape covering each channel region of the other transistor areas;

(h) by using said second gate electrode layer and said first gate electrode layer as a mask, implanting first high concentration impurity ions into the n-channel transistor areas to form high impurity concentration source/drain regions;

(i) by using said second gate electrode layer as a mask, etching said first gate electrode layer;

(j) forming a fourth mask exposing the CMOS p-channel transistor area and covering at least a gate electrode area in the area of the n-channel transistor with the LDD regions;

(k) implanting second high concentration p-type impurity ions having a concentration lower than the first high concentration to form high impurity concentration source/drain regions in the p-channel transistor area;

(l) by using said fourth mask as an etching mask, etching said second gate electrode layer to pattern a gate electrode of the n-channel transistor with the LDD regions; and

(m) implanting low concentration n-type impurity ions to form the LDD regions of the n-channel transistor with the LDD regions.

8. The manufacture method for a thin film transistor substrate according to claim 7, wherein the CMOS n-channel transistor has no LDD regions and said third mask has a gate electrode shape above the CMOS n-channel transistor.

9. The manufacture method for a thin film transistor substrate according to claim 7, wherein said fourth mask has a shape covering the CMOS n-channel transistor area.

10. The manufacture method for a thin film transistor substrate according to claim 7, wherein said step (a) comprises the subsidiary steps of:

(a1) depositing said semiconductor layer on the substrate in an amorphous phase;

(a2) implanting p-type impurity ions into said semiconductor layer at an impurity concentration which sets the threshold voltage suitable for the p-channel transistor; and

(a3) applying a laser beam to said semiconductor layer to change the amorphous phase to a polycrystallized phase.

11. The manufacture method for a thin film transistor substrate according to claim 7, wherein said first and second gate electrode layers have different etching characteristics.

12. The manufacture method for a thin film transistor substrate according to claim 7, wherein said first gate electrode layer is a refractory metal layer and said second gate electrode layer is an aluminum alloy layer.

13. The manufacture method for a thin film transistor substrate according to claim 7, further comprising the steps of:

(l) forming a first interlayer insulating film covering said three types of thin film transistor structures;

(m) forming contact holes through said first interlayer insulating film and said gate insulating film;

(n) forming a conductive layer on said first interlayer insulating film, said conductive layer covering said contact holes;

(o) pattering said conductive layer to form electrodes and wiring lines;

(p) forming a second interlayer insulating film covering said electrodes and said wiring lines;

(q) forming contact holes through said second interlayer insulating film;

(r) forming a transparent electrode layer on said second interlayer insulating film, said transparent electrode layer covering said contact holes; and

(s) patterning said transparent electrode layer to form a transparent electrode of each pixel.

14. A thin film transistor substrate comprising:

a substrate;

a first transistor structure having a first semiconductor layer formed on said substrate, a first gate insulating film and a first gate electrode, wherein a channel region of said first semiconductor layer under said first gate electrode is intentionally doped with only p-type impurities, said first semiconductor layer includes n-type LDD regions outside the channel region and high impurity concentration n-type source/drain regions outside the n-type LDD regions, and said first gate electrode is made of a lamination of a first metal layer and a second metal layer;

a second transistor structure having a second semiconductor layer formed on said substrate, a second gate insulating film and a second gate

electrode, wherein a channel region of said second semiconductor layer under said second gate electrode is intentionally doped with only p-type impurities, said second semiconductor layer includes high impurity concentration n-type source/drain regions outside the channel region, and said second gate electrode is made of a lamination of said first metal layer and said second metal layer; and

a third transistor structure having a third semiconductor layer formed on said substrate, a third gate insulating film and a third gate electrode, wherein a channel region of said third semiconductor layer under said third gate electrode is intentionally doped with p-type impurities and n-type impurities, said third semiconductor layer includes high impurity concentration p-type source/drain regions outside the channel region, and said third gate electrode is made of said second metal layer.

15. The thin film transistor substrate according to claim 14, wherein said second semiconductor layer has n-type LDD regions outside the channel region, and the high impurity concentration n-type source/drain regions outside the n-type LDD regions.

16. The thin film transistor substrate according to claim 14, wherein said first and second metal layers have different etching characteristics.

17. The thin film transistor substrate according to claim 16, wherein said first metal layer is a refractory metal layer and said second metal layer is an aluminum alloy layer.

18. A thin film transistor substrate comprising:

a substrate;

a first transistor structure having a first semiconductor layer formed on said substrate, a first gate insulating film and a first gate electrode, wherein a channel region of said first semiconductor layer under said first gate electrode is intentionally doped with only p-type impurities, said first semiconductor layer includes n-type LDD regions outside the channel region and high impurity concentration n-type source/drain regions outside the n-type LDD regions, and said first gate electrode is made of a second metal layer;

a second transistor structure having a second semiconductor layer formed on said substrate, a second gate insulating film and a second gate electrode, wherein a channel region of said second semiconductor layer under said second gate electrode is intentionally doped with p-type impurities at the first impurity concentration, said second semiconductor layer includes high impurity concentration n-type source/drain regions outside the channel region, and said second gate electrode is made of said second metal layer; and

a third transistor structure having a third semiconductor layer formed on said substrate, a third gate insulating film and a third gate electrode, wherein a channel region of said third semiconductor layer under said third gate electrode is intentionally doped with p-type impurities at a second impurity concentration lower than the first impurity concentration, said third semiconductor layer includes high impurity concentration p-type source/drain regions outside the channel region, and said third gate electrode is made of a first metal layer different from said first metal layer.

19. The thin film transistor substrate according to claim 18, wherein said second semiconductor layer has n-type LDD regions outside the channel region, and the high impurity concentration n-type source/drain regions outside the n-type LDD regions.

20. The thin film transistor substrate according to claim 18, wherein said first metal layer has etching characteristics different from those of said second metal layer.

21. The thin film transistor substrate according to claims 20, wherein said first metal layer is a refractory metal layer and said second metal layer is an aluminum alloy layer.